Programmable 360° Inclinometer

Silicon Anomaly

ADIS16203

ADIS16203 ANOMALIES

This anomaly list describes the known bugs, anomalies, and workarounds for the ADIS16203.

Analog Devices, Inc., is committed, through future silicon revisions, to continuously improve silicon functionality. Analog Devices tries to ensure that these future silicon revisions remain compatible with your present software/systems by implementing the recommended workarounds outlined here.

ANOMALY STATUS

Reference Number	Description	Status
er001	Manual Flash®/EE memory update failures	Fixed
er002	ALM_SMPL1/ALM_SMPL2 write causes device failure	Fixed
er003	Invalid orientation bit not active	No fix

MANUAL FLASH/EE MEMORY UPDATE FAILURES [er001]

Background	The ADIS16203 uses a dual memory structure to maintain its operational configuration. The RAM register structure controls the operation of the device, and the Flash/EE memory contents determine what is loaded into the RAM at startup and during reset recovery events. The Flash/EE memory is updated by using a control bit in the COMMAND register of this part.
Issue	Flash/EE memory update fails at a rate of approximately 5%.
Workaround	Date Code 0722 and older can exhibit this behavior. Verification: Check lower four bits of Address 0x52. If $\geq$ 3, then the update is validated. If the updates cannot be verified using the above criteria, the STATUS register's Flash Memory error flag can be used to check for this condition. If the error flag indicates a failure, perform another Flash/EE update (COMMAND register) and then verify using the STATUS register again. Given the lower failure rate, two attempts should be sufficient.
Related Issues	None.

ALM_SMPL1/ALM_SMPL2 WRITE CAUSES DEVICE FAILURE [er002]

Background	The ALM_SMPL1 and ALM_SMPL2 registers provide critical timing configuration data for rate-of-change alarm settings, which are limited to the lower byte of each register. The upper bytes of these registers are documented as not used.
Issue	Writing to the upper byte of these registers causes a device failure.
Workaround	Date Code 0805 and older can exhibit this behavior. Verification: Check lower four bits of Address 0x52. If $\geq$ 4, then the update is validated. If the updates cannot be verified using the above criteria, do not write to Address 0x25 and Address 0x27. If they are accidentally written to, then a power cycle or reset is required to restore normal operation.
Related Issues	None.

INVALID ORIENTATION BIT NOT ACTIVE [er003]

Background	In the ADIS16203 data sheet, Revision 0, Table 19 describes Bit 6 in the STATUS register as an error flag for invalid orientation. The original purpose of this function was to validate the vertical position of the ADIS16203. The ADIS16203 accuracy specifications are dependent on vertical alignment.
Issue	This function is not supported in the current device configuration.
Workaround	Do not use this function in the ADIS16203. The next generation product in this family (ADIS16209) will provide the necessary features to support vertical alignment verification.
Related Issues	None.

Rev. 0

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